Enhanced controller for a four-leg inverter operating in a stand-alone microgrid with unbalanced loads

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ABSTRACT

Stand-alone low voltage (LV) microgrids supplying small local loads far from the utility grid are becoming an increasingly popular alternative to a total reliance on the centralized utility grid. In most of LV microgrids, three-phase four-wire distribution systems are used to supply both single- and three-phase loads. Unequal distribution of loads can result in voltage unbalance problems. The use of the four-leg inverter is one of the best solutions for providing a neutral current path and compensating unbalanced load conditions in standalone LV microgrids. This paper proposes a fast control technique to compensate unbalanced voltage conditions for a four-leg inverter operating in a stand-alone LV microgrid. The suggested technique provides the current controller's orthogonal component without introducing any additional dynamics or distortions. The major benefits of the recommended per-phase control technique over conventional orthogonal signal generation (OSG) methods are enhanced steady-state and dynamic performances as well as independency to the system parameters. Several simulation results are provided to confirm the superior performance of the suggested methods.

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1. INTRODUCTION

A microgrid contains distributed generators (DGs), power electronic devices, storages, and sensitive loads that can operate in both grid-tied and islanded (stand-alone) modes [1]. Under islanding operation, at least one of the DG units must work in the grid-forming mode to provide voltage and frequency stability [2]. This voltage and frequency control can be accomplished by inverter-based DGs, synchronous machines, or other types of generators [3].

Most three-phase islanded microgrids feed unbalanced and/or nonlinear loads [4]. The existence of single-phase loads in a three-phase microgrid can cause excessive neutral current, reactive power burden, and unbalanced voltage conditions. However, power quality is highly important for sensitive loads in islanded microgrids. Therefore, it is necessary to provide high power quality voltages in stand-alone microgrids [5], [6].

The provision of the neutral wire has become an obligation for three-phase microgrids supplying unbalanced loads. There exist multiple ways to provide a neutral wire in microgrids. Soto *et al.* [7], used a three-phase conventional (three-leg) inverter, connecting its output to a Δ -Y transformer to provide the neutral wire. This method is expensive compared to other methods and causes excessive copper and magnetic

losses [3]. Using a transformer will make the circuit bulky due to the low frequency of the output voltage and current. Furthermore, using a split dc-link capacitor is proposed in the literature [3], [8]. Balancing the dc voltage on capacitors, when injecting unbalanced currents, can cause problems in the control procedure. Moreover, capacitors' capacities change differently over time and this can complicate the problem. Another method for providing the neutral wire is to use a four-leg inverter [9]. In this type of inverter, two switches are added to the three-phase conventional inverter which forms the fourth leg [10]. The neutral wire is connected to the middle of the fourth leg. This method does not have the disadvantages mentioned above, i.e. it is not expensive, it is less bulky, the efficiency is high, and balancing the capacitors' voltages is not an issue anymore [3].

The output voltage of the inverter must have a ripple-free voltage; hence, a low pass filter must be used to block the switching frequency harmonics and pass the fundamental frequency [11]. There are several types of power filters that block the switching frequency [12]. The most known ones are the L, LC, and LCL filters [13]. L and LCL filters are generally used when the purpose is to control the output current. However, since we aim to control the output voltage, the LC filter is an appropriate choice.

Various types of switching methods are also proposed to control the switches of all four legs [14], [15]. Three-dimensional space vector modulation (3-D SVM) is one of the most common methods used for this approach[10]. Some factors that have made this method so popular are low output voltage/current distortion, high utilization of the dc-link voltage, the ability to minimize switching losses. Despite its popularity, this method needs complex calculations for choosing the switching vectors. Another technique for controlling the switches is to use the carrier-based pulse-width modulation (PWM) method which is proposed in [15]. It was also proved to be equivalent to the 3-D SVM technique, but it is simpler to implement.

For using the PWM method, one needs a carrier signal and a voltage signal. The voltage signal is the output of the controller which can come in different types. Well-known controllers that are used for controlling an inverter are hysteresis controller [16], deadbeat (DB) controller [17], finite-control-set modelpredictive control (FCS-MPC) [18], sliding mode control (SMC) [19], proportional-integral (PI) [20] and proportional resonant (PR) controller [21]. Variable switching frequency and high current ripple are the major boundaries with hysteresis control. The problem of the chattering phenomenon in discrete implementation is the main disadvantage of the SMC. Predictive control is difficult and involves a lot of calculations. On the other hand, PR controllers are normally used for sinusoidal reference voltages yet, even PR controllers are unable to fully eliminate the steady state error of a sinusoidal control signal. In order to overcome this problem, one can use PI controllers with dc signals, because PI controllers can completely track dc reference signals. One way to convert the AC waveforms into dc ones is to use Park transformation [22]. The output of this transformation, the dq signals are dc values and can be controlled by PI controllers. However, when the three-phase signals become unbalanced, the dq signals will not be pure dc anymore. A double-frequency ripple will be added to both d and q axes. Hence, PI controllers cannot properly control the signals and the steady-state error will not be zero. The PI controller has good performance by tuning the parameters for first-order and second-order systems; nonetheless, it becomes more difficult for higher order systems and it is tuned by try and error. The fuzzy-PID controller has shown good performance in these situation [23].

Several methods have been proposed to eliminate this ripple. One of them is to utilize low-pass filters, but this method decreases the response time [24]. Another method is to first calculate the symmetrical components and then use the Park transformation [25]. Since the symmetrical components are balanced, the output of the abc-dq transformation will be pure dc. The disadvantage of this method is that calculating symmetrical components is based on implementing a time-domain delay to the signals. This delay is modeled as an all-pass filter in the frequency-domain. Therefore, it will be difficult to include the symmetrical components calculators (SCCs) in the small-signal model [26].

In this paper, a fast control approach for a four-leg inverter in the islanded mode under unbalanced conditions is proposed. On the outer voltage loop, a second-order generalized integrator (SOGI) is used to create the α and β components from the real signals. However, using this technique in the current controller introduces undesired delays. In this paper, a fast and robust method is used to create the orthogonal signal for the current control loop. This method does not impose any delays to the system and also it is not dependent on the system parameters.

The paper is structured as shown in: Section II is associated with modeling the three-phase four-leg inverter and its mathematical equations. The third section describes the proposed control technique in this paper in detail. The simulation results under different scenarios are given in section IV and it is shown that this technique can provide balanced voltages in highly unbalanced conditions. Finally, the conclusion is provided.

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2. THREE-PHASE FOUR-WIRE INVERTER MODEL

2.1. Topology

Configuration of the three-phase four-leg inverter with an output LC filter is shown in Figure 1. As shown in this Figure, an ideal battery is used to simulate the dc-link voltage which simplifies the analysis. Moreover, to control the zero-sequence current, an additional fourth leg is connected to the conventional three-phase inverter. The additional fourth leg increases the number of gating signals and thus the control complexity. However, the for-leg inverter can handle balanced or unbalanced loads and linear or nonlinear loads. The inductor used in the fourth leg, as well as the inductors in the other legs, minimizes the switching frequency ripples.



Figure 1. Four-leg inverter with loads

2.2. Mathematical model

The voltage of each phase in Figure 1 is obtained using Kirchhoff's voltage law to the three-phase four-leg inverter as shown in (1):

$$e_{abc_f} = \left(R + L\frac{d}{dt}\right)i_{L_abc} + v_{abc_n} - \left(R + L\frac{d}{dt}\right)i_n \tag{1}$$

where $e_{abc_f} = [e_{af}, e_{bf}, e_{cf}]^T$, $v_{abc_n} = [v_{an}, v_{bn}, v_{cn}]^T$ and $i_{L_abc} = [i_{La}, i_{Lb}, i_{Lc}]^T$ represent the input voltage, output voltage, and inductor current, respectively. I_n is also defined as the neutral current. Furthermore, by applying Kirchhoff's current law in Figure 1, the following equations are obtained:

$$i_{L_abc} = C \frac{d}{dt} v_{abc_n} + i_{0_abc}$$
⁽²⁾

$$i_n = i_{La} + i_{Lb} + i_{LC} \tag{3}$$

where $i_{O_abc} = [i_{Oa}, i_{Ob}, i_{Oc}]^T$ represents the load current.

As shown in (1)-(3) represent the system model in the abc frame. Using the Park transformation, the dq0 frame model of the system is given by (4) and (5).

$$\begin{cases} E_d = V_d + \left(R + L\frac{d}{dt}\right)I_d - L\omega I_q \\ E_q = V_q + \left(R + L\frac{d}{dt}\right)I_q - L\omega I_d \\ E_0 = V_0 + \left(R + L\frac{d}{dt}\right)I_0 \end{cases}$$

$$\begin{cases} I_{Ld} = C\frac{d}{dt}V_d + I_{Od} - C\omega V_q \\ I_{Lq} = C\frac{d}{dt}V_q + I_{Oq} + C\omega V_d \\ I_{L0} = C\frac{d}{dt}V_0 + I_{O0} \end{cases}$$
(5)

where ω is the coordinate angular frequency for the Park transformation. Park transformation matrix is shown in (6):

$$T = \frac{2}{3} \begin{bmatrix} \cos(\theta) \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$
(6)

To design the system controller and analyze the stability of the inverter, the per-phase method can be used [27]. Here the single-phase inverter representation of the four-leg inverter is used for design and analysis [28]. The per-phase model for one phase to the neutral point of a four-leg inverter is demonstrated in Figure 2. According to this figure, I_L and V_C are inductor current and capacitor voltage, respectively. Input voltage and the load connected to that phase are represented as an ideal control voltage source and current source, respectively.

Figure 3 depicts the small-signal block diagram of the inverter with output LC filters. The block diagram is in the dq frame. Control of signal in the synchronous reference frame is so easy with PI controllers; because PI controllers have a simple implementation. As it is shown, one pair coupling exists in this figure while they omitted by feed-forwards that's design in the Figure 4. So, control of the system is well done in dq frame without any coupling and d and q components are controlled independently.



Figure 2. Per-phase/single-phase representation of an inverter



Figure 3. Small signal block diagram of the grid-forming inverter with output LC filter

3. THE PROPOSED CONTROL TECHNIQUE

3.1. Per-phase controller

The control block diagram of the three-phase four-leg inverter is shown in Figure 4. As it is shown in this figure, this controller includes a cascaded voltage control loop and a current control loop to compensate unbalanced voltage conditions in a stand-alone LV microgrid. Also, V_{Ca} and I_{La} represent the capacitor voltage and inductor current of the output filter of phase a, respectively. V_{α} and I_{α} are the same as V_{Ca} and I_{La} . V_{β} is the orthogonal component of V_{α} . V_{β} is attained from the SOGI block [29]. SOGI is one of the OSG types and its structure is represented in Figure 5. As it is shown in Figure 5, the SOGI consists of two integrators that result slow dynamic responses (In Figure 5, k is set to 1 in this work). In order to obtain a better dynamic response, a faster method is needed to compute the orthogonal component. For solving this problem, the article uses another OSG method that is explained in section B and I_{β} is obtained from this method. The most important difference between Figure 4 and the block diagram shown in [28] is the method of obtaining the I_{β} that has no dependency on the grid's parameters. After the OSG blocks, the d and q components of the capacitor voltage, inductor current, and output current are attained by the park transformation blocks. It is needed to provide a synchronous reference frame in order to use simple controllers like Fuzzy-PIDs to regulate the reference values. The PI controller gains were designed as done in [28] and the Fuzzy-PID were designed as done in [23]. Eventually, E_{α} is equal to the E_a fed into the PWM block, while E_{β} is discarded. As shown in Figure 4, two feed-forward (FF) blocks are used in both the current controller and the voltage controller loops. The main purpose of these four FF blocks is to compensate the coupling between the d and q axes. Moreover, $\sin\theta$ and $\cos\theta$ values are needed for converting ac voltages and currents into dc ones. Since the inverter is working in the grid-forming mode, $\sin\theta$ and $\cos\theta$ values are known and they do not need to be measured or calculated.



Figure 4. Block diagram of the proposed per-phase controller



Figure 5. SOGI block diagram

If the inverter were supposed to connect to a grid and inject current, it would be necessary to measure θ using a phase locked loop (PLL) and calculate $\sin\theta$ and $\cos\theta$ values. Therefore, in this situation, the small-signal model of the PLL should also be added to the system which causes delays. By using this method each phase is controlled independently with any extra dynamics into the current control loop and finally, the unbalanced load voltages are compensated in the best way.

3.2. The proposed OSG technique

The OSG used in this paper generates an orthogonal current (I_{β}) . The idea of this method has been proposed in [27], but it is used in another topology of the inverter and another topology of the grid. As it is shown, one of the fastest alternatives for the SOGI is the OSG depicted in Figure 6.

This technique is applied in the four-leg inverter for computing the β axis of the load current. Using this method, the reference values of the load currents, I_{α} and I_{β} , are obtained from (7) and (8), respectively [27].

 I_q^* .

$$I_{\alpha}^{*} = B \sin(\varphi + \gamma) \tag{7}$$

$$I_{B}^{*} = B\cos(\varphi + \gamma) \tag{8}$$

where, B, γ and ϕ are as shown in (4)-(5),

$$B = \sqrt{I_d^{*2} + I_q^{*2}}$$
(9)

$$\gamma = tan^{-1} \begin{pmatrix} I_q^* \\ I_d^* \end{pmatrix} \tag{10}$$

$$\varphi = \int \frac{t}{0} \omega(\tau) d\tau \tag{11}$$

By using (7)-(11), the beta component of the reference current is generated as a function of I_d^* and

The advantage of this method is its independence on the grid's parameters such as the inductance or resistance of the output filter. Also, this method does not add any distortion and dynamics to the system and generates the orthogonal component very fast, while the SOGI has an inherent delay in generating the beta component. Eventually, the output current response is fast and smooth and the load voltage is constant under balanced and unbalanced loads.



Figure 6. Block diagram of the used OSG to obtain I_{β}

3.3. PWM Technique

Fuzzy-PID controllers in the current control create the reference signals. Then these signals are transformed back to the abc frame. In the next step, the abc signals are imported to the PWM block to create the switching signals and produced the three-phase reference voltages of the inverter. The carrier-based PWM method has been used in this research for the generation of the inverter output voltages [14]. This method has been applied because of its strong performance and simple implementation. The block diagram of carrier-based PWM is presented in Figure 7.



Figure 7. Block diagram of carrier-based PWM

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 e_{af} , e_{bf} , and e_{cf} are inputs of the α component obtained from the four-leg inverter. They can be represented as (12).

$$\begin{cases} e_{ao} = e_{af} + e_{fo} \\ e_{bo} = e_{bf} + e_{fo} \\ e_{co} = e_{cf} + e_{f0} \end{cases}$$
(12)

where, 'o' stands for the fictive midpoint of the dc-link and e_{fo} is the offset voltage that is calculated as shown in (13),

$$e_{fo} = mid\left(-\frac{e_{max}}{2}, -\frac{e_{min}}{2}, -\frac{e_{min}+e_{min}}{2}\right)$$
(13)

where e_{fo} corresponds to the medium value of the mentioned variables. Also, e_{max} and e_{min} correspond to the maximum and minimum instantaneous values of e_{af} , e_{bf} , and e_{cf} respectively. They are also represented in (14) and (15),

$$e_{max} = max(e_{af}, e_{bf}, e_{cf}) \tag{14}$$

$$e_{min} = min(e_{af}, e_{bf}, e_{cf}) \tag{15}$$

And their constraints are represented as (16),

$$-V_{dc} \le e_{af}, e_{bf}, e_{cf} \le V_{dc} \tag{16}$$

Also, the ON-times of the upper switches of the respective legs can be achieved from (17).

$$\begin{cases} T_a = \frac{T_s}{2} + \frac{e_{ao}}{v_{dc}} T_s \\ T_b = \frac{T_s}{2} + \frac{e_{co}}{v_{dc}} T \\ T_c = \frac{T_s}{2} + \frac{e_{co}}{v_{dc}} T \\ T_f = \frac{T_s}{2} + \frac{e_{do}}{v_{dc}} T \end{cases}$$
(17)

where T_s is the period of the triangular carrier signal.

4. SIMULATION AND RESULTS

The average model of the three-phase four-leg inverter shown in Figure 1 has been simulated in MATLAB/Simulink software. Then, the performance of the transient and steady-state response of the suggested control method is tested and evaluated when different loads are connected to the stand-alone grid. At last, the performance of the offered technique is compared with the conventional method [26] and fictive axis emulation (FAE) method [28]. System parameters under study are indicated in Table 1.

Table 1. System parameters under study

Variable description	Value			
DC link voltage	460 [V]			
Load voltage	180 [V]			
Filter capacitor	25 [µF]			
Filter inductor	3 [mH]			
The internal resistance of filter ind	0.1 [Ω]			
Grid frequency	60 [Hz]			
Switching scheme	carrier-based PWM			
FF1 gain		$2*\pi^{*}60^{*}25^{*}10^{-6}$		
FF2 gain		$2^{*}\pi^{*}60^{*}3^{*}10^{-3}$		
Reference voltages	V_d^*	220 [V]		
	V_q^*	0 [V]		
PI voltage controller gains	Prop. (K _p)	1		
	Integ. (K _i)	1		

Three different scenarios for loading conditions are considered. At first, the four-leg inverter supplies a resistive balanced load ($R_a = R_b = R_c = 10.75 [\Omega]$). Next, at 0.3 [s], an inductive load is added between phases B and C (R=30 [Ω] and L=15 [mH]), and finally, at 0.5s, a resistive load is added on phase C (R=15 [Ω]). Figure 8 illustrates the output waveform of the load voltages and current in the abc frame for all three methods. Figures 8 (a)-(c) is also depicted the unbalanced load condition that is happened in 0.3 [s], when an inductive load is added between phases B and C. Also, the results of the proposed technique are compared with the FAE method [28] and conventional technique [26]. It is observed that the waveforms of all control methods remain balanced in steady-state at all the various load conditions that are considered in this study. However, as seen, the transient response of the proposed method is faster than the two other conventional methods. In addition, the proposed method is compensated for two phase unbalances with smaller disturbance.

Figure 9 also depicts the output voltage and current waveforms of the inverter for unbalanced load conditions. In this test, a resistive load is added on phase C (R=15 Ω) at 0.5 [s]. Figures 9 (a) depicts the voltages and currents of the conventional method, respectively. Figures 9 (b) also show the voltages and currents of the FAE method, Figures 9 (c) illustrates voltages and currents of the suggested method, respectively. As can be seen, the transient response of the proposed method is so faster than the FAE and conventional methods, and the load voltage is compensated under highly unbalanced conditions.



Figure 8. Output voltage and current waveforms of the inverter for unbalanced load condition at t=0.3[s]; (a) conventional technique voltage and current, respectively; (b) FAE technique voltage and current, respectively; and (c) the proposed technique voltage and current, respectively



Figure 9. Output voltage and current waveforms of the inverter for unbalanced load condition at t=0.5[s]; (a) conventional technique voltage and current, respectively; (b) FAE technique voltage and current, respectively; and (c) the proposed technique voltage and current, respectively

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The reference and actual waveforms of voltage in phases A, B, and C for the grid-forming inverter in the q and d components are depicted in Figure 10 and Figure 11, respectively. Figure 10 (a)-(c) demonstrated the obtained q voltage components of phase A, B and C via the FAE method and proposed method, respectively and Figures 11 (a)-(c) depicted obtained d voltage components of phase A, B and C via the FAE method and proposed method, respectively. By comparing the proposed method's operation with the FAE method one can better observe in this article's scheme is the better speed of transient response rather than the FAE to following load changes. Deviations in the voltage waveforms are also shorter and smaller.

The reference and actual waveforms of current in phases A, B, and C for the grid forming inverter in the q and d components are depicted in Figure 12 and Figure 13, respectively. Figure 12 (a)-(c) demonstrated the obtained q current components of phase A, B and C via the FAE method and proposed method, respectively and Figure 13 (a)-(c) depicted obtained d current components of phase A, B and C via the FAE method and proposed method, respectively. As can be seen, the reference current following in the proposed method is so faster than the FAE and its deviation is so shorter and smaller. Fast transient response is the result of the proposed method.



Figure 10. Comparison between the q components of the reference voltage waveform (V_q^*) with actual voltage waveform (V_q) in three-phase. (a) phase A with FAE technique and proposed technique, respectively; (b) phase B with FAE technique and proposed technique, respectively; and (c) phase C with FAE technique and proposed technique, respectively



Figure 11. Comparison between the d components of the reference voltage waveform (V^{*}_d) with actual voltage waveform (V_d) in three-phase. (a) phase A with FAE technique and proposed technique, respectively; (b) phase B with FAE technique and proposed technique, respectively; and (c) phase C with FAE technique and proposed technique, respectively



Figure 12. Comparison between the q components of the reference current waveform (I_q^*) with actual current waveform (I_q) in three-phase. (a) phase A with FAE technique and proposed technique, respectively; (b) phase B with FAE technique and proposed technique, respectively; and (c) phase C with FAE technique and proposed technique, respectively

Table 2 shows the total harmonic distortion (THD) for all three load combinations and the Phase Voltage Unbalance Rate (PVUR) that are tested in steady-state. They are all evaluated for the proposed technique, the FAE, and the conventional OSG methods. Based on IEEE Std 141, PVUR is [30]:

$$\% PVUR = \frac{maximum \ voltage \ deviation \ from the \ average \ phase \ voltage}{average \ phase \ voltage} \times 100$$
(18)

According to IEEE's recommendation, the value of PVUR should be less than 2% for the system's distribution. As shown in Table 2, the THD and PVUR of the voltages are quite low when the proposed control method is used, for example, PVUR in the unbalanced#1 scenario improved 98 and 99 percent relative to the FAE and conventional methods, respectively. Also, the THD of the phase B voltage in the same scenario improved 82% and 92% with respect to the FAE and conventional methods, in sequence.



Figure 13. Comparison between the d components of the reference current waveform (I_d) with actual current waveform (I_d) in three-phase. (a) phase A with FAE technique and proposed technique, respectively; (b) phase B with FAE technique and proposed technique, respectively; and (c) phase C with FAE technique and proposed technique, respectively

Table 2. Simulation results												
Load type	Conventional method				FAE method			Proposed method				
		THD(%)	DVIID		THD(%)				THD(%)			
	Phase	Phase	Phase	(%)	Phase A PhaseB	DhasaD	Phase	Phase (%)	PhaseA	Phase Phase	Phase	(%)
	А	В	С			Phaseb	С			В	С	
Balanced	0.94	1.24	1.13	0.104	0.50	0.52	0.52	0.040	0.05	0.04	0.07	0.001
Unbalanced#1	1.32	2.41	2.52	0.652	0.51	1.83	1.83	0.100	0.03	1.59	1.59	0.003
Unbalanced#2	3.48	3.05	3.45	0.611	1.16	1.23	2.83	0.312	0.02	0.22	1.92	0.005

5. CONCLUSION

An improved per-phase control strategy for a grid-forming four-leg inverter using a fast orthogonal signal generation (OSG) technique operating under unbalanced conditions is suggested in this paper. The use of the new OSG technique allows the four-leg inverter to provide balanced output voltages under unbalance load conditions without introducing any extra dynamics into the current control loop and distortions into the generated orthogonal signal. The suggested controller has presented outstanding voltage control performance, such as fast transient response and tiny steady-state error under unbalanced load conditions. In addition, its operation does not depend on the system parameters. The superior performance of the suggested technique is shown using simulation studies under various scenarios.

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